AMENDMENTS TO THE SPECIFICATION

Please amend the paragraphs at page 2, line 10 to page 3, line 3, as follows:

In this manufacturing method, the holes are formed by irradiating a laser beam on the insulating resin layer on the connection pads, after sealing the semiconductor chip with the insulating resin. Such a laser processing, however, can cause [[a]] damage in the semiconductor chip. Furthermore, the laser processing cannot contribute to making the semiconductor chip smaller, or to giving the connection pads on the semiconductor chip with a [[more]] narrower pitch.

Further, JP 2001-15650 A also discloses a technique of forming a hole in an insulating resin layer by using chemical developing.

A strong etching material is usually used as a developer to etch an epoxy resin generally used as the insulating resin. It is, however, difficult to use a strong etching material because such a strong material causes [[a]] damage in a semiconductor chip. It is therefore extremely difficult to form holes having a high aspect ratio in the processed hole. That is, it is extremely difficult to make holes having a numeric value found by dividing the hole depth by a diameter of the largest opening portion. Accordingly, the hole forming process by using a chemical development on an epoxy resin that is on a semiconductor chip cannot contribute to giving the connection pads on the semiconductor chip a [[more]] narrower pitch.

Please amend the paragraph at page 5, lines 13-25 as follows:

Further, because the through hole is formed as mentioned above ~~abave~~, it becomes easy to form the through hole having an aspect ratio equal to or greater than one (where the term aspect ratio denotes a value in which the depth of the through hole

is divided by a reduced radius of a surface that is parallel to an opening surface of the through hole, and that has a maximum surface area). A semiconductor chip or a semiconductor device possessing a connecting conductor formed by embedding a conductor in this through hole can prevent signal interference between the semiconductor chip and wirings, and between adjacent conductors, from occurring, even if connection pads are given a narrow pitch.

Please amend the paragraph at page 10, lines 7-15 as follows:

It is preferable that an upper side surface of the insulating layer 14, which is a wiring support, be flat in this case because the build-up multi-layer substrate is disposed on the insulating layer 14. Preferably, the flatness of the upper side surface is equal to or less than 10 μm [[? m]]. If there is a portion having flatness greater than 10 μm [[? m]] in the upper side surface, the wirings of the build-up multi-layer substrate formed on the portion can break more easily.

Please amend the paragraph at page 14, lines 23-26 as follows:

Heat treatment is performed next for 10 minutes at 110° [[110? C]] as a pre-bake, thus forming a layer of the photosensitive resin 202 having a film thickness on the order of 70 μm [[? m]].

Please amend the paragraph at page 15, lines 19-26 as follows:

A light from a mixture of g, h, and i rays is irradiated at 1,000 mj/cm^2, thus performing light exposure. Development is then performed for 190 to 210 seconds at a temperature of 23°C [[23? C]] by using a developer (PD523) made from an aqueous

solution that contains 2.38% tetramethyl ammonium hydroxide. Washing is then performed for 120 seconds by using ultra purified water, thus the resist posts 204 being formed.

Please amend the paragraph at page 16, lines 1-15 as follows:

Referring to FIG. 2D, the semiconductor chip 205 is next joined to the support member 207 through the peelable adhesive 206. A foaming peelable sheet in which a joining force reduces due to foaming by heating to a temperature equal to or greater than a specific temperature may also be used for the peelable adhesive 206. In addition, adhesives that are made from materials having a particularly high solubility, or which easily swell, in a specific solvent compared to other materials of the semiconductor device manufactured by the method of manufacturing below may also be used. For example, silicone adhesives and the like, which have a particularly high solubility in solvents such as toluene, may be used. Alternatively, a [[an]] porous adhesive layer may be used. The porous adhesive layer sponges a solvent, thus dissolving easily.

Please amend the paragraph at page 20, lines 1-10 as follows:

The resist posts 204 are removed by immersing the manufacturing process piece shown in FIG. 2F in a liquid that contains from 96% to 99% dimethyl sulfoxide and 1% tetramethyl ammonium hydroxide (THB-S1), or a liquid that contains from 89% to 95% dimethyl sulfoxide and from 1 to 3% tetramethyl ammonium hydroxide (THB-S2) for 5 to 10 minutes at a temperature of 50°C to 70°C ~~50? C to 70? C~~, followed by washing. Ultrasonic vibration may also be added to the piece through the liquid at the same time is immersed in the liquid.

Please amend the paragraphs beginning at page 21, line 4 as follows:

The wiring conductor 211 and the connecting conductor 212 may be formed by using different processes. Both are formed by using the same process in this embodiment, however. The wiring conductor 211 and the connecting conductor 212 thus form a substantially continuous body, and joining interfaces do not exist in any conductor. The development of contact resistance, signal reflection, and the like originating in the joining interface are prevented by thus not forming joining interfaces. The semiconductor device manufactured by the processes described above has little generation of noise or heat, and supports a [[more]] narrower pitch. Further, the number of process steps decreases by forming the two conductors in a lump, and this contributes to an increase in productivity in the method of manufacture, an increase in yield, and a reduction in cost of the manufactured product.

Electroplating is used as a method of forming the wiring conductor 211 and the connecting conductor 212 at the same time in this embodiment. Compared to other formation methods, electroplating has high manufacturing efficiency. The thickness of the wiring conductor 211 is set on the order of 10 μm [[? m]] in this embodiment. The thickness of about 10 μm [[? m]] prevents breaking of wirings within the build-up multi-layer substrate 214 due to a step between the wirings and substrate 214 from occurring for cases in which the build-up multi-layer substrate 214 is formed directly on the insulating layer 210 that is provided with the wirings 213 based on the wiring conductor 211.

Please amend the paragraph at page 24, lines 25-30 as follows:

In addition, at least a portion of the wiring 15 is embedded in the insulating layer 14. In this embodiment, a step between the wirings 15 and a surface of the

insulating layer 14 that is opposite to a surface facing the semiconductor chip 11 is smaller than the step in the first embodiment, for example equal to or less than 10 μm [[? m]].

Please amend the paragraph at page 27, lines 25-26 as follows:

FIG. 4B-2 shows an example of the second embodiment in which the insulating member 210 has a concave shape.

Please amend the paragraph beginning at page 30, line 29 as follows:

A specific example of a method of making the insulating layer by transfer molding is shown here. A movable male die and a movable female die are contacted by adding pressure, thus forming a void portion (cavity) in which the insulator 210 is formed. With the cavity in a residually heated state, a thermosetting epoxy resin is supplied from one side of the mold, for example from the female die side, at an injection force of 80 kg and an injection velocity of 1.2 mm/s. The resin supplied within the cavity is then held for 90 seconds by a metal mold temperature of 175°C to 180°C ~~175? C to 180? C~~, thus set and forming the insulator 210 within the cavity. The mold is cooled next, and then opened. The insulator 210 is then taken out of the mold.

Please amend the paragraph at page 33, lines 1-22 as follows:

Basically ~~Basicaly~~, the material is selected by considering the characteristics that must be satisfied as a semiconductor device part. That is, the material is selected by considering electrical characteristics such as dielectric characteristics and insulating characteristics, thermal characteristics such as the withstand temperature, the thermal expansion coefficient, and the thermal conductivity, and in addition, the moisture

absorption characteristics and the like. In addition, the through holes 209 and the wiring grooves 303 are formed in the insulator 210 in this embodiment, and therefore the material is selected while considering processability. For cases where cutting, grinding, or micro-punching is performed, a relatively hard resin like a phenol resin may be used from the viewpoint of increasing processing precision. Alternatively, a sintered ceramic such as alumina or zirconia may be used. For cases in which laser processing is performed, the processing efficiency increases by using a material having a large absorption in the wavelength which the laser light has. For example, the processing precision increases if a material such as polyimide or polysulfone is employed when using an excimer laser.

Please amend the paragraph at page 35, lines 13-21 as follows:

The wirings 213 and the insulator 210 are made of different materials here, and thus their removal processing rates differ. Accordingly, a small step develops between the wirings 213 and the insulator 210 in the processed surface after removal. In order to prevent a wiring within the multi-layer substrate from breaking, it is preferable that the step be equal to or less than 10 μm [[? m]] for cases in which a build-up multi-layer substrate is formed on the insulator 210.

Please amend the paragraph at page 40, lines 24-28 as follows:

FIG. 7A shows a state where the semiconductor chip 205 provided with the first resist posts 204 on the connection pads 203 is joined to the support member 207 through the peelable adhesive 206. Second resist ~~resisit~~ posts 700 are also disposed on the support member 207.

Please amend the paragraph at page 51, lines 12-20 as follows:

It is preferable that steps between the exposed surface of the insulating layer 210 and the wirings 213 be equal to or less than 10 μm [[? m]] in height at this point. This is because there is a possibility that the build-up multi-layer substrate will be formed directly contacting the insulating layer 210 in this embodiment, and the likelihood that wire breakage will occur in wirings within the build-up multi-layer substrate increases for cases where the step is greater than 10 μm [[? m]].